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FPGA Hardware Implementation of DOA Estimation Algorithm Employing LU Decomposition
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Abstract
In this paper, authors present their work on field-programmable gate array (FPGA) hardware implementation of proposed direction of arrival estimation algorithms employing LU factorization. Both L and U matrices were considered in computing the angle estimates. Hardware implementation was done on a Virtex-5 FPGA and its experimental verification was performed using National Instruments PXI platform which provides hardware modules for data acquisition, RF down-conversion, digitization, etc. A uniform linear array consisting of four antenna elements was deployed at the receiver. LabVIEW FPGA modules with high throughput math functions were used for implementing the proposed algorithms. MATLAB simulations of the proposed algorithms were also performed to validate the efficacy of the proposed algorithms prior to hardware implementation of the same. Both MATLAB simulation and experimental verification establish the superiority of the proposed methods over existing methods reported in the literature, such as QR decomposition-based implementations. FPGA compilation results report low resource usage and faster computation time compared with the QR-based hardware implementation. Performance comparison in terms of estimation accuracy, percentage resource utilization, and processing time is also presented for different data and matrix sizes. © 2013 IEEE.

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